Claims

[c1] What is claimed is:

1. A routing method for routing a plurality of signal traces out of a plurality of corresponding bumper pads in a multi-layer circuit board, the multi-layer circuit board comprising at least a first layer and a second layer, the method comprising:

arranging the plurality of bumper pads based on a plurality of triangle units;

routing a plurality of signal traces out of a plurality of corresponding bumper pads of in the first layer;

routing a plurality of signal traces out of a plurality of corresponding bumper pads in the second layer not to be vertically parallel with the plurality of signal traces routed in the first layer; and

arranging a plurality of shielding traces among the plurality of signal traces in the first layer and in the second layer.

[c2] 2. The routing method of claim 1, wherein the multi-layer circuit board further comprises a third layer used as a ground plane so that the plurality of shielding traces are connected to the third layer.

[c3] 3. The routing method of claim 2, wherein the second layer is vertically underneath the first layer, and the third layer is vertically underneath the second layer.

[c4] 4. The routing method of claim 1 being applied to a flip chip packaging technique, a wire bondingtechnique, a tape automatic bondingtechnique, and other packaging techniques.

[c5] 5. A tile-based routing method for routing a plurality of signal traces out of a plurality of corresponding bumper pads in a multi-layer circuit board, the multi-layer circuit board comprising at least a first layer and a second layer, the method comprising:
arranging the plurality of bumper pads as a bumper-tile block by a specific forming process;
assigning a plurality of signal traces corresponding to a plurality of bumper pads of the bumper-tile block as a plurality of first-layer traces being routed in the first layer;
assigning a plurality of signal traces corresponding to a plurality of bumper pads of the bumper-tile block as a plurality of second-layer traces being routed in the second layer;
routing the plurality of first-layer traces straight forward;
routing the plurality of second-layer traces with a turn not to be vertically parallel with the plurality of first-layer traces; and
shielding the plurality of first-layer traces and the plurality of second-layer traces.

[c6] 6. The tile-based routing method of claim 5 further comprising:
arranging a first-layer shielding trace between every two adjacent first-layer traces in the first layer of the multi-layer

circuit board; and

arranging a second-layer shielding trace between every two adjacent second-layer traces in the second layer of the multi-layer circuit board.

[c7] 7. The tile-based routing method of claim 6, wherein the multi-layer circuit board further comprises a third layer used as a ground plane, the method further comprising:

utilizing each first-layer shielding trace connected to the third layer for grounding; and

utilizing each second-layer shielding trace connected to the third layer for grounding.

[c8] 8. The tile-based routing method of claim 7, wherein the second layer is vertically underneath the first layer, and the third layer is vertically underneath the second layer.

[c9] 9. The tile-based routing method of claim 5, wherein each bumper-tile block comprises 8 bumper pads, which correspond to 8 signal traces capable of carrying 8 input/output signals, organized in a plurality of triangle units with equal length of each side.

[c10] 10. The tile-based routing method of claim 9, wherein the bumper-tile block is positioned in a periphery area of a die.

[c11] 11. The tile-based routing method of claim 5 being applied to a flip chip packaging technique and other packaging techniques.

[c12] 12. The tile-based routing method of claim 5, wherein the multi-layer circuit board is a 6-layer build-up substrate or any other multi-layer board for high pin-count application.

[c13] 13. A method for routing a plurality of signal traces out of a plurality of corresponding bumper pads for implementation of a die on a multi-layer circuit board, the method comprising:

utilizing the plurality of bumper pads positioned in a periphery area of the die;

utilizing a plurality of power/ground bumper pads positioned in a center area of the die;

arranging the plurality of bumper pads in a specific forming process;

assigning a plurality of signal traces corresponding to a plurality of bumper pads as a plurality of first-layer traces being routed in a first layer of the multi-layer circuit board;

assigning a plurality of signal traces corresponding to a plurality of bumper pads as a plurality of second-layer traces being routed in a second layer of the multi-layer circuit board wherein the second layer is vertically beneath the first layer;

routing the plurality of first-layer traces straight away from the die;

routing the plurality of second-layer traces with a turn not to be vertically underneath the first-layer traces; and

shielding the plurality of first-layer traces and the plurality of

second-layer traces by routing a plurality of shielding traces out of the plurality of power/ground bumper pads.

[c14] 14. The method of claim 13, wherein the plurality of signal traces are capable of carrying a plurality of input/output signals for communicating the die with a plurality of exterior devices installed on the multi-layer circuit board.

[c15] 15. The method of claim 13, wherein the plurality of bumper pads can be grouped into a plurality of bumper-tile blocks.

[c16] 16. The method of claim 15, wherein each bumper-tile block comprises 8 bumper pads organized in a plurality of triangle units with equal length of each side.

[c17] 17. The method of claim 13, wherein the plurality of shielding traces comprise a plurality of first-layer shielding traces routed in the first layer and a plurality of second-layer shielding traces routed in the second layer.

[c18] 18. The method of claim 17 further comprising:
arranging each first-layer shielding trace between every two adjacent first-layer traces in the first layer of the multi-layer circuit board; and
arranging each second-layer shielding trace between every two adjacent second-layer traces in the second layer of the multi-layer circuit board.

[c19] 19. The method of claim 18, wherein the multi-layer circuit board further comprises a third layer used as a power/ground plane, the method further comprising:
utilizing each first-layer shielding trace connected to the third layer for grounding; and
utilizing each second-layer shielding trace connected to the third layer for grounding.

[c20] 20. The method of claim 13, wherein the multi-layer circuit board is a 6-layer build-up substrate or any other multi-layer board for high pin-count application.

[c21] 21. The method of claim 13 being applied to a flip chip packaging technique and other packaging techniques.